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ORIGINAL RESEARCH ARTICLE

FinFET based SRAM cells design in various topologies using different power reduction techniques

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ABSTRACT

In Very Large Scale Integration (VLSI) design, device scaling is restricted due to subthreshold swing limitations and short channel effects. This article discusses the role of different power reduction techniques in the implementation of 14 nm fin-shaped field-effect transistor (FinFET) centered static random access memory (SRAM) cells with good subthreshold swing and reduced short channel effects (SCE). Dynamic threshold and power gating are incorporated in SRAM cells to advance the memory cell performance by reducing static power dissipation in standby mode. The power analysis was performed on different SRAM cells with different transistor count i.e., 6, 7, 8, and 9. The performance of SRAM cell is analysed in power dissipation and is reduced by 20% using power gating method and in dynamic threshold it is reduced to nano watts due to less leakage power.

Keywords: FinFET; SRAM cell; power reduction techniques

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1. Introduction

In current microprocessors, memory arrays composed of SRAM cells take up a huge amount of chip space. It's also to blame for the chip's astronomically high power consumption[1]. According to previous reports, the read and writing data consume up to 70% of the active power during switching.

Using more modern complementary metal-oxide-semiconductor (CMOS) technology to take benefit of their tiny size and lower operating voltages is one technique to reduce power[2]. Conventional CMOS technology nodes experience challenges i.e., threshold voltage reduction[3]. Several SRAM designs for power reduction have been presented in recent decades. The three primary design strategies are current adjustment, supplementary supply, current-mode sense amplifier[4]. Two inverters are cross linked to custom a latch in an SRAM cell. Transistors M1 and M2 connect the latch to the two-bit line[5]. Under the control of the word line, M1 and M2 can be switched open or closed. The switches M1 and M2 are closed in read mode by activating word line signal. As a result, Q and Q_bar are always complementary to one another as shown in **Figure 1**. The operation of the SRAM cell is given in **Table 1**.

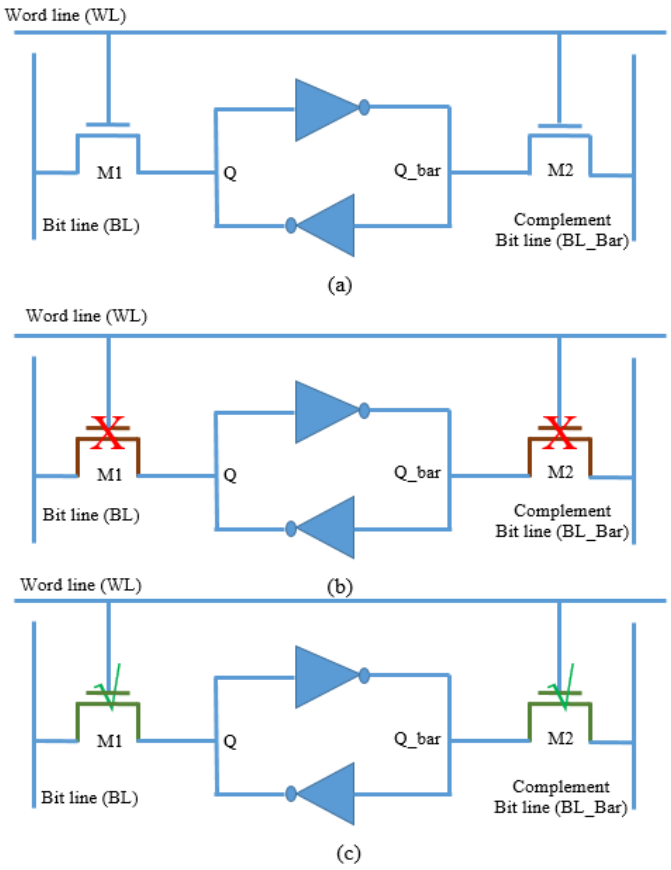


Figure 1. SRAM cell, **(a)** basic model; **(b)** hold mode M1-OFF & M2-OFF; **(c)** read, write mode M1-ON & M2-ON.

Table 1. Basic SRAM cell operations.

Operation	Q	Q_bar	Word line (WL)	M1	M2	BL	BL_bar	Sense amplifier output
Hold	0	1	0	OFF	OFF	-	-	-
	1	0	0					
Read	0	1	1	ON	ON	VDD/2	VDD/2	0 (BL < BL_bar)
	1	0	1					1 (BL > BL_bar)
Write	0	1	1	ON	ON	VDD/2	GND	1
	1	0	1					0

The write mode at the end of the two-bit line keeps track of their status and adjusts the output accordingly. Instead of sensing the condition of bit lines BL and BL_Bar, the write circuit drives them during write operation[6]. It activates the word line by placing the proper value on bit line BL and its complement on bit line BL_Bar. When the word line is deactivated, the cell is forced into the matching state, which it retains. However, all have various problems[7]. The development of FinFET devices alleviated many of these issues, as FinFET has many benefits over CMOS, with minimum leakage[8].

This research presents a column gate-control mechanism that uses 14 nm FinFET innovation to minimize the power consumption required for SRAMs. The word-line selects a minimum supply in ideal condition, minimizing standby power dissipation. The efficiency and usability of the basic techniques are verified on Silicon. The basic power reduction techniques utilized in SRAM cell design are shown in **Figure 2**.

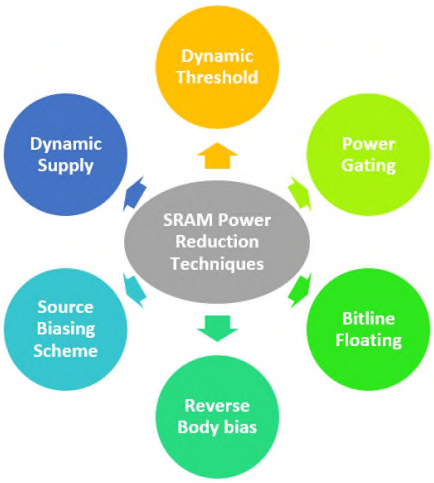


Figure 2. SRAM cell power reduction techniques.

2. Related work

The development of energy-efficient systems has become a main requirement as a result of the rapid rise of the Internet of things (IoT), which is expected to be the next main outlook of the electronics industry[9]. Because static random access memories (SRAMs) account for roughly 90% of the floor area of recent processors used in the development of IoT technology, they are regarded as the primary source of total power efficiency and, as a result, energy efficiency[10]. The traditional 6T SRAM consist of two pairs of inverters and two n-type metal-oxide-semiconductor field-effect transistors (MOSFETs). In the sub-threshold region, this cell exhibits poor read static noise margin (RSNM), as a quantity of reading permanency, or write static noise margin (WSNM), due to competing for read-write demands[11]. As a result, it is unable to function at an ultra low voltage (ULV) to even further reduce power usage. An 8T SRAM future increases the cell's efficiency by using transmission gates as switch devices in place of the n-type MOSFETs used in a typical 6T cells. This is illustrated by the transmission gate's capacity to propagate strong logic values. In evaluation to a regular 6T cell, the typical 8T presented in uses two additional n-type MOSFETs, one read word line, and one read bit line to conduct its read function. This separates data-storage nodes from bit lines during reading operations, improving cell RSNM at the expense of overhead space. Furthermore, read path leakage is a significant problem for the traditional 8T SRAM cell. With the advancement of technology, this problem becomes even more serious. The same bit lines are used for both reads and write operations in the completely differential 9T SRAM cell built-in. Due to the doubling of the number of transistors attached to the same bit lines, the overall bit lines capacitance increases, resulting in a high read delay and power factor[12]. To reduce leakage and improve RSNM, the SRAM cells presented employ a modified form of reading access buffer. A brief review in the design of FinFET based SRAM cell is given in **Table 2**.

Table 2. Review on FinFET based SRAM cells.

Reference No.	Description	Performance indices	Limitations
[13]	Designed a 6T SRAM cell using 10 nm FinFET. Primarily discussed about power, performance and area.	Failure bit count, power.	Proper power analysis was not performed.
[14]	A broad range fixed current-free current mirror-based LS for near-threshold operation with logic error detection.	Delay, power	SRAM design is not validated with proper SNR analysis.
[15]	Improved read speed and minimal leak in a multiple monolithic transistor 8T SRAM cell.	Leakage current power	Power reduction techniques are not incorporated.
[16]	This paper's key advancement is to offer a picture of these consequences on SRAM as a technology scale.	Delay	Used conventional design approaches.
[17]	8T FinFET SRAMs are more capable of near-threshold functioning than 6T FinFET SRAMs. Back gates in opposite way inverters reduce leakage and power while increasing SNM.	SNM	Power analysis was not discussed.

A short overview on SRAM cells power reduction strategies is described in **Table 3**.

Table 3. Review on SRAM cells power reduction techniques.

Reference No.	Power reduction technique	Description	Observations
[18]	Resonant supply boost-in	Resonant voltage boosting in a reduced voltage SRAM.	Supply voltage is dynamic.
[19]	Biasing scheme	A PDP mitigation circuit for a mono reduced power 16 nm FinFET 6T SRAM architecture.	Dynamic voltage is applied to the body terminal.
[20]	Dynamic threshold	Development of a Schmitt -trigger-based SRAM cell with reduced, variation-resilient IoT based applications.	One dynamic threshold transistor was used.
[21]	Bit-line floating	Bulk-CMOS and FinFETs are used to create an 8T reduced and low-leakage half-selection error-free.	Bit-line floating
[22]	Reverse body bias	SRAMs with dynamic energy-quality governance regarding.	Complimentary voltage is applied to the body.
[23]	Power gating	Low-energy functioning using a power-gated 9T architecture.	Two sleep transistors are loaded in conventional SRAM cell.

3. Problem statement

High level device scaling has caused in enlarged short-channel effects and statistical variability in device characteristics (SCEs)[24]. SCEs can be improved by using a thinner gate oxide. Thinner gate oxide, on the other hand, causes exponentially more gate leakage. As a result, numerous potential transistor architectures have researched to substitute bulk MOSFETs to overcome SCE. FinFETs are one of them, and they're thought to be a good fit for mounted CMOS. FinFETs are more resistant to SCE because the gate voltage has superior control over the channel. Moreover, by systematizing the metal gate work function, the threshold voltage (V_{th}) can be easily regulated[25]. Furthermore, due to nearly intrinsic channel doping, V_{th} changes caused by arbitrary dopant variation in the channel region are decreased. Because memories account for 80% of the device area in high-performance, high-efficiency, and very resilient SRAMs are required. Unfortunately, process variations impair SRAM read and write stabilities in scaled technologies, mainly in scaled supply voltages. Because a memory array contains a large number of tiny transistors, process differences can cause read, write, and access failures, especially at reduced supply voltages[26]. In addition, in traditional 6T cell, the struggle between reading and writing stabilities is an inescapable design limitation that exacerbates the impact of process changes on efficiency. The solution to the above mentioned problem is summarized in **Table 4**.

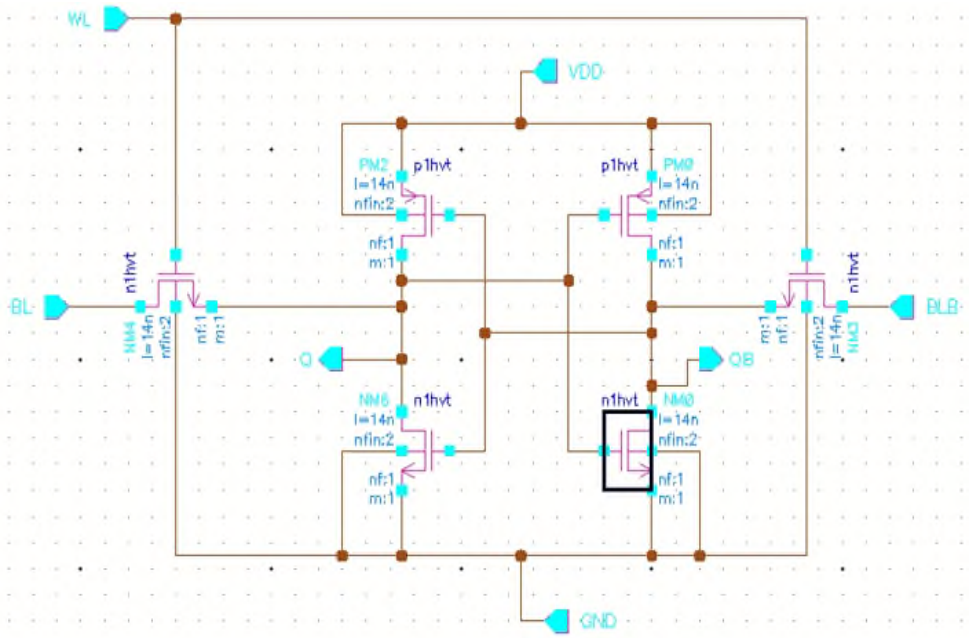
Table 4. Problem statement.

Research challenge	Description	Techniques
Power reduction	The present embedded systems IC's demands low power SRAM cells with high efficiency.	Dynamic threshold & power gating

4. SRAM cells using FinFETs

Over the last five decades, technology scaling dynamic factor behind the exponential rise in transistor sum, better efficiency, and lower cost. FinFETs, a kind of multi-gate transistor, has surpassed conventional MOSFETs in terms of performance, short-channel behaviour, and power dissipation[27]. FinFETs offer more control over the channel because they surround it on all sides. This minimizes the leakage current by overwhelming the drain-induced barrier lowering effect, improving the sub-threshold slope, and suppressing the drain-induced barrier dropping effect. FinFETs also use a lightly doped or un-doped channel to minimize random doped oscillations. FinFETs scaling is getting increasingly difficult due to lithography's nearing limits, unbearable short-channel effects, and rising production costs. The Silicon (Si) fin is the vertical structure that

serves as the channel in the FinFET. SiO_2 is the gate oxide, a dielectric material that electrically isolates the gate from the channel. Hafnium Dioxide (HfO_2) is a high-k dielectric material used in modern transistors to reduce leakage and improve performance. Polysilicon is used as the gate material. The channel length is 14 nm is the distance between the source and the drain. Fin Width of 8 nm, Fin Height is 22 nm. The aspect ratio of 2.75, the aspect ratio describes the proportion of the fin's height to its width. Other methods, such as the creation of new cell, the use of new organizational methods, the development of new designs, and unique processing models, are required to continue to improve technology. 14 nm FinFET based SRAM cell in different topologies such as 6T,7T, 8T and 9T are shown in parts **(a), (b), (c)** and **(d)** of **Figure 3** respectively.



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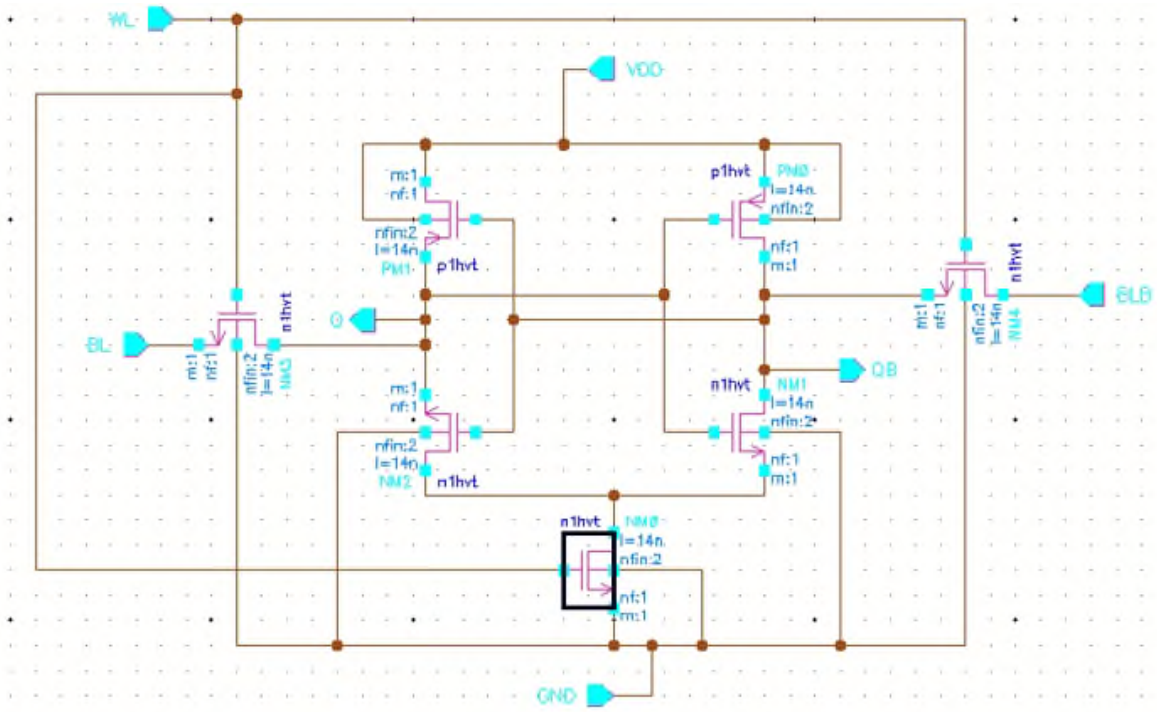
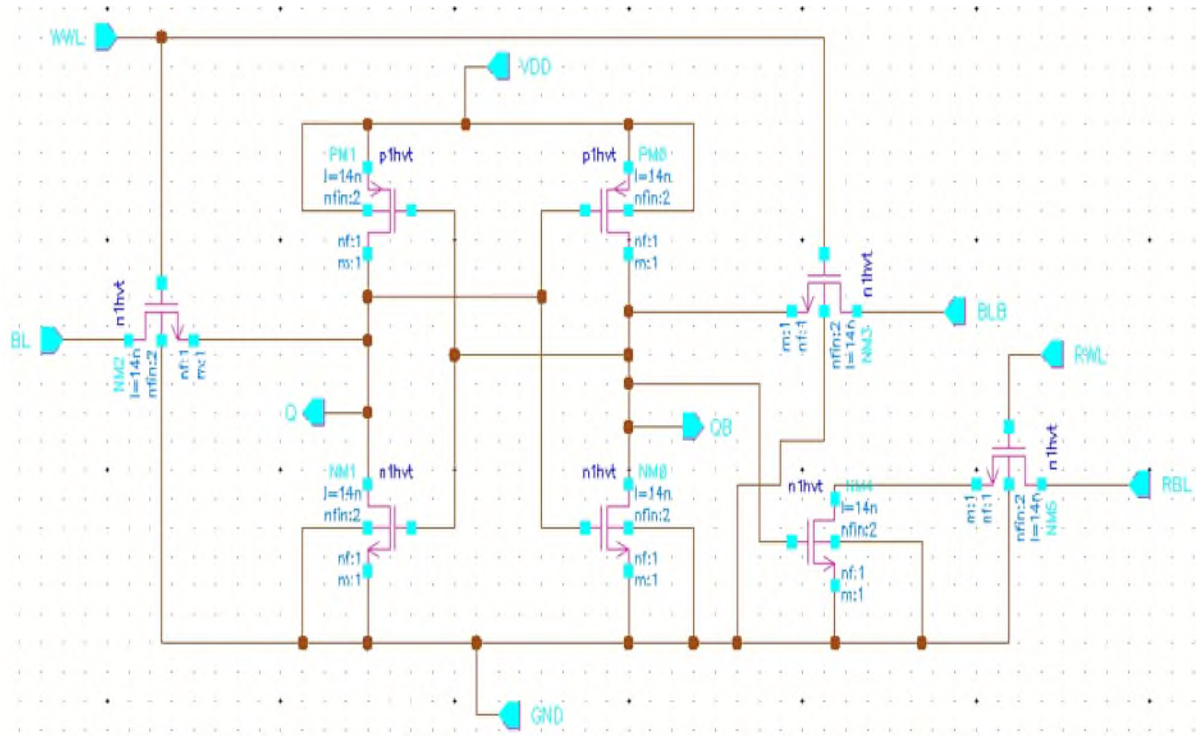


(b)

Figure 3. (*Continued*).



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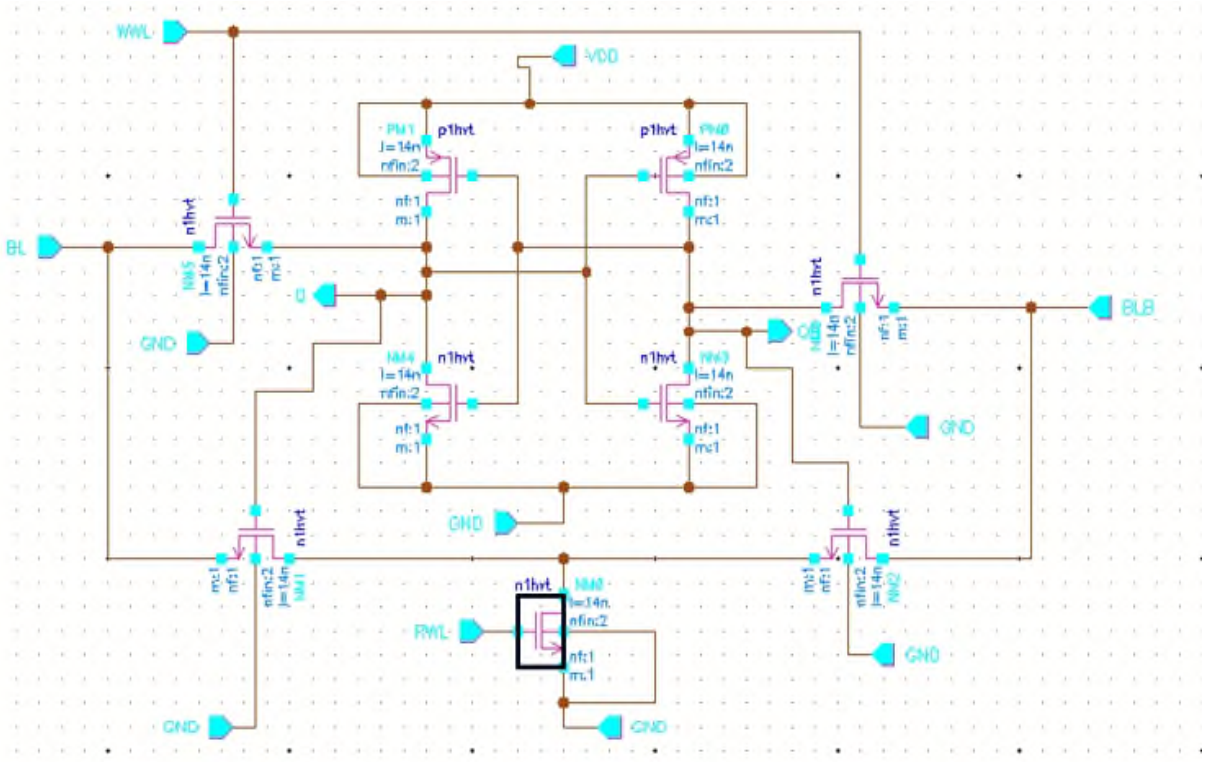


(d)

Figure 3. SRAM cells with 14 nm FinFET, **(a)** 6T cell; **(b)** 7T cell; **(c)** 8T cell; **(d)** 9T cell.

The transient analysis of 6T SRAM cell is shown in **Figure 4**. The static noise margin (SNM) curves of 6T SRAM cell for read, write and hold operations are given in parts **(a)**, **(b)**, **and (c)** of **Figure 5** respectively. The performance of SRAM cell in different topologies is analyzed and the same is presented in **Table 5**.

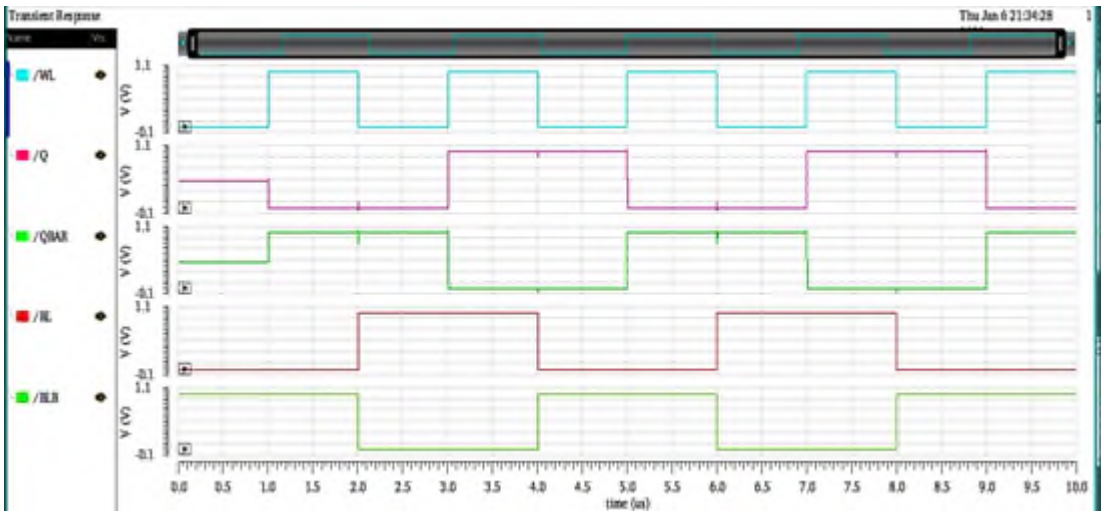
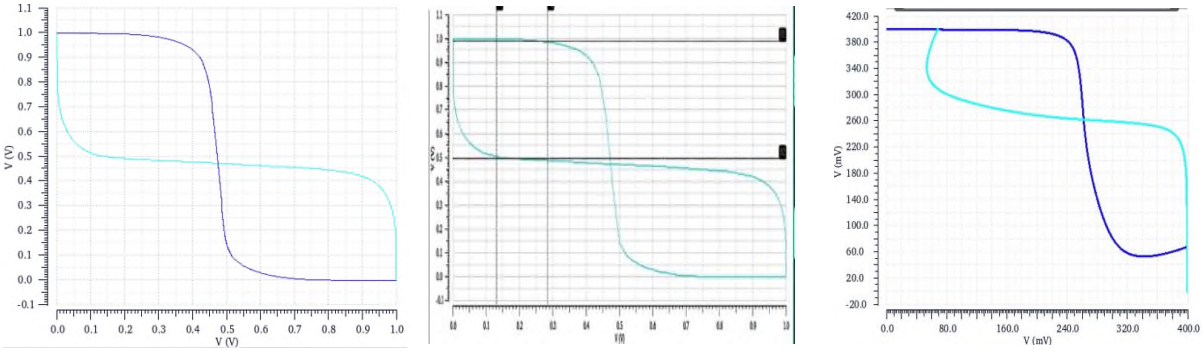


Figure 4. 6T SRAM write signals.



(a) **(b)** **(c)**

Figure 5. SNM curves of 6T SRAM cell **(a)** write; **(b)** hold; **(c)** read.

Table 5. Comprehensive analysis on different SRAM cells.

Parameter	**Number of FinFETs**			
	6T	**7T**	**8T**	**9T**
Power (W)	17.05×10^{-6}	15.22×10^{-6}	25.57×10^{-6}	20.88×10^{-6}
SNM (mV)	Hold = 480.85 Read = 483.88 Write = 480.99	Hold = 480.85 Read = 483.88 Write = 480.99	Hold = 480.85 Read = 483.88 Write = 480.99	Hold = 480.85 Read = 483.88 Write = 480.99
Data retention voltage (mV)	473.8×10^{-3}	505.6×10^{-3}	512.5×10^{-3}	473.8×10^{-3}
Propagation delay (ns)	9.60	9.58	9.58	9.56

4.1. Dynamic threshold

There's real bias in the form of a body impact in the dynamic threshold body of a M_DT because the body and gate contacts are attached together[28]. It constantly modifies the transistors' threshold voltages, which implies that if the gate voltage changes, the substrate voltage changes as well, resulting in a difference in the threshold voltage. M_DT's behaviour can be compared to that of a regular FinFET when the gate voltage is zero. The pictorial representation of dynamic threshold technique based 6T topology SRAM cell is depicted in **Figure 6**. 14 nm FinFET based SRAM cell with dynamic threshold technique in different topologies such as 6T,7T, 8T and 9T are shown in parts **(a)**, **(b)**, **(c)** and **(d)** of **Figure 7** respectively.

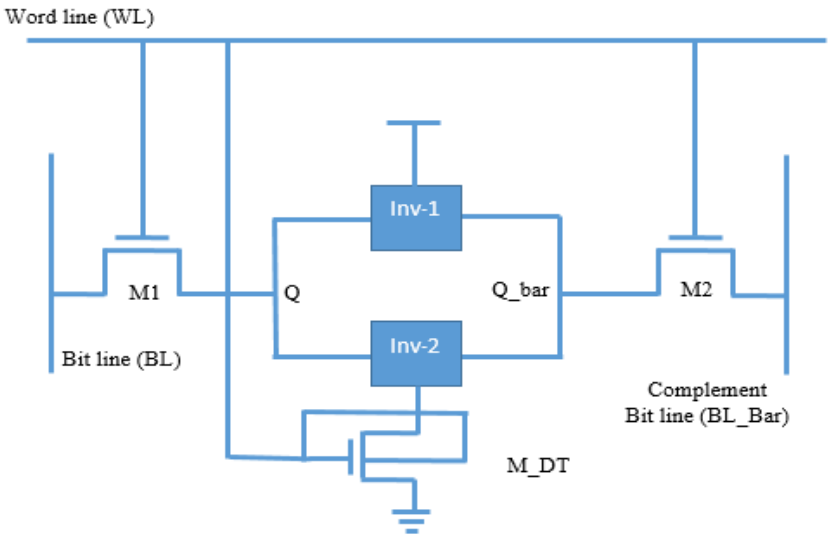
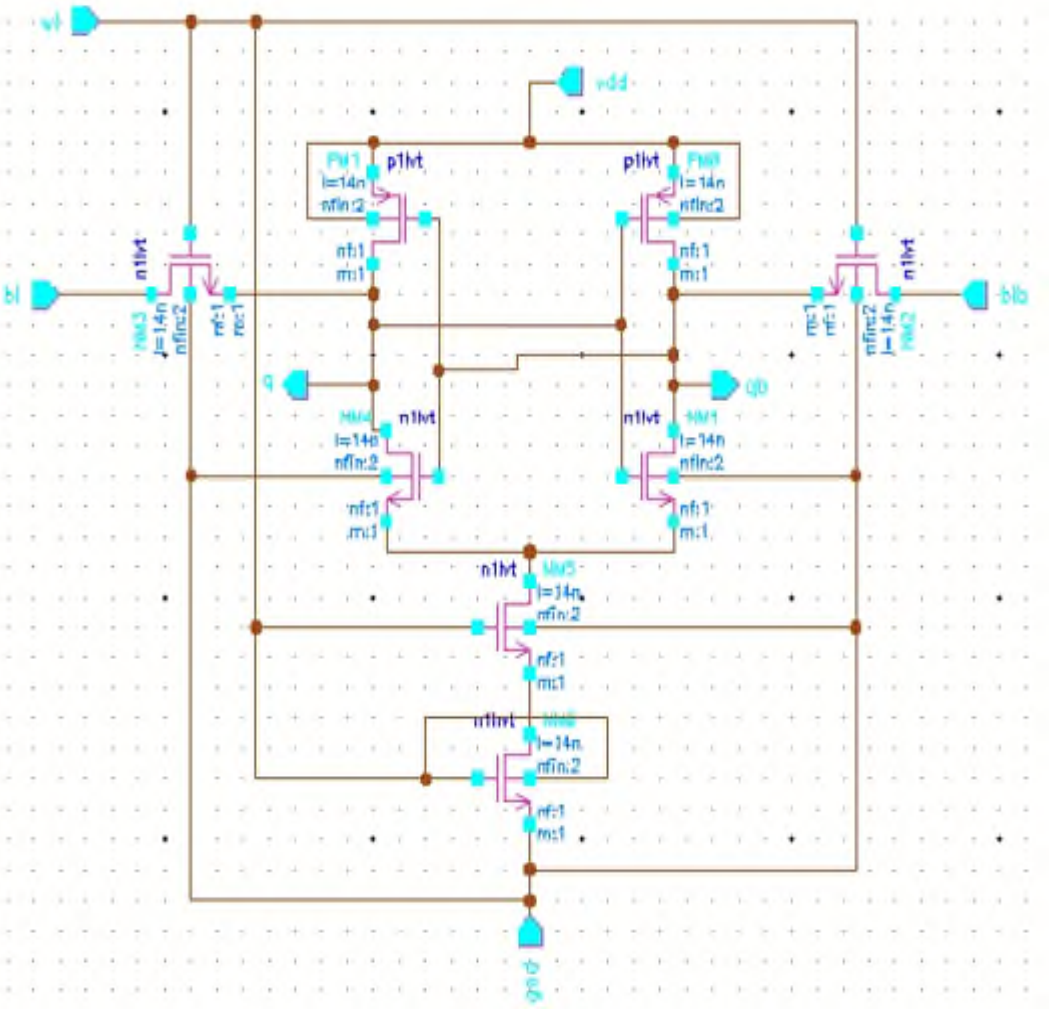
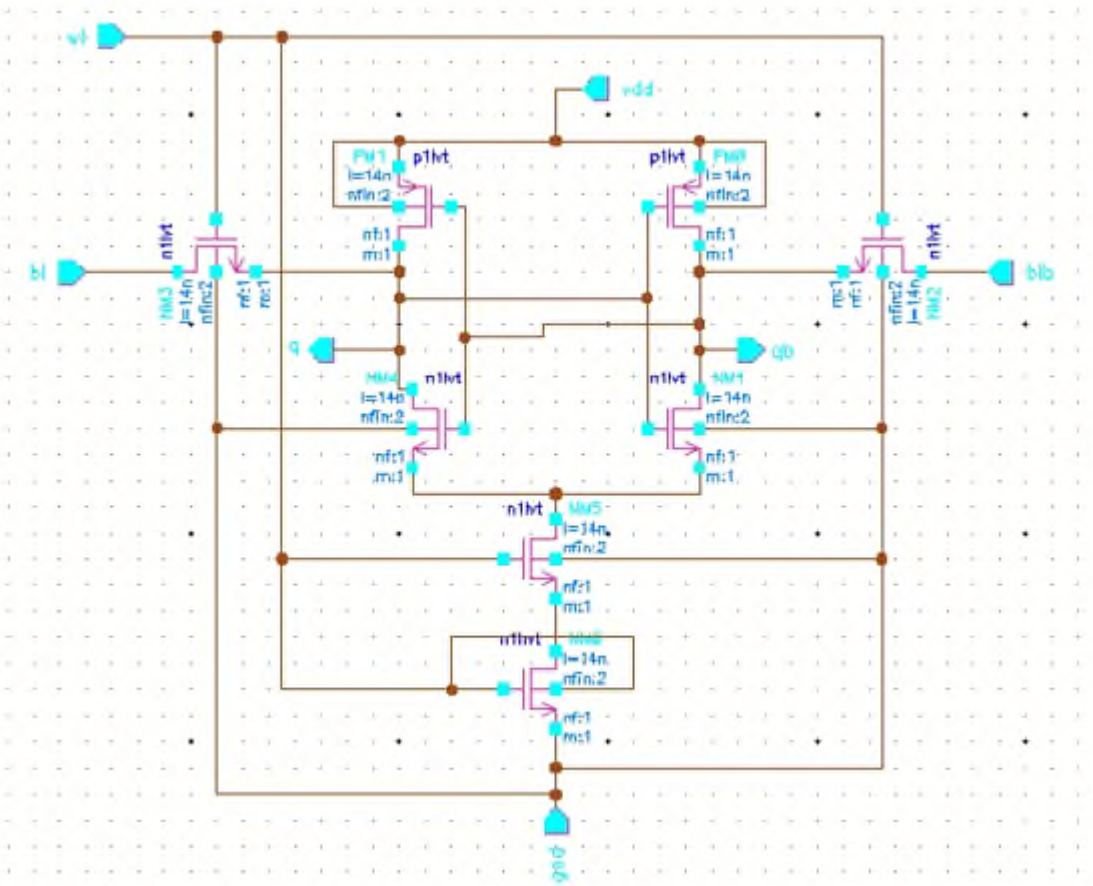


Figure 6. SRAM with dynamic threshold technique.



(a)

Figure 7. (*Continued*).



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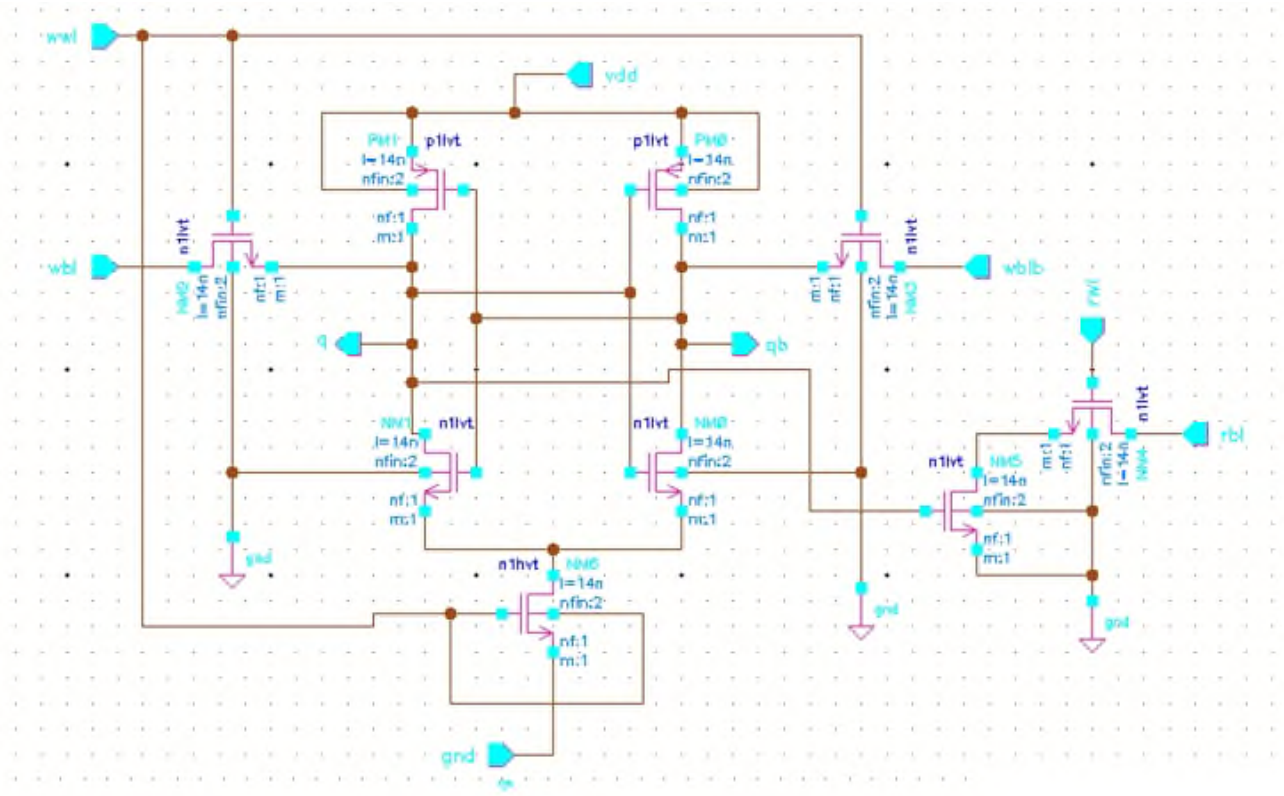
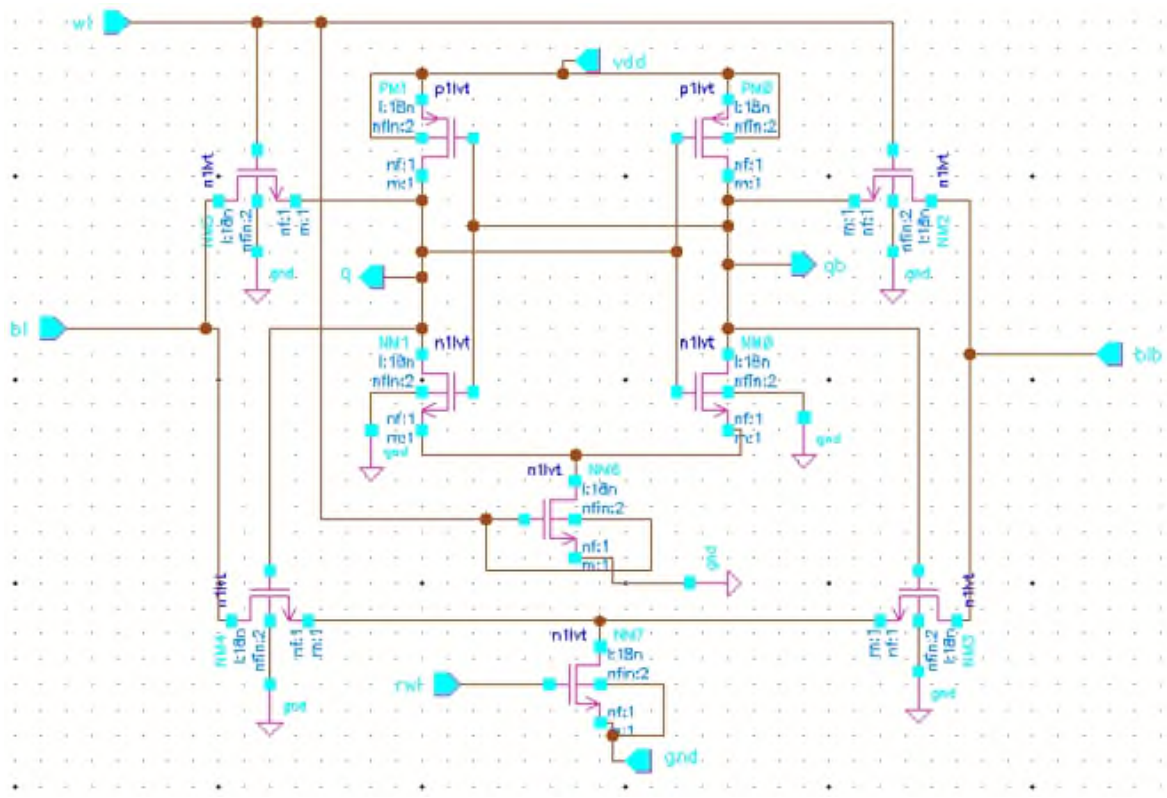


(c)

Figure 7. (*Continued*).



(d)

Figure 7. SRAM cells with dynamic threshold, **(a)** 6T cell; **(b)** 7T cell; **(c)** 8T cell; **(d)** 9T cell.

4.2. Power gating

In power gating technique two smart transistors are added between supply voltage (VDD) and ground (GND) at top and bottom of cross coupled inverter pair which reduces the leakage power consumption of the SRAM memory cell in hold mode of operation. Power and delay are optimized with the help of power gating[29]. Power gating is possible with incorporation of sleep transistor (or) variable body bias. In this paper, the role of sleepy transistor in achieving low power was analysed. In power gating a high-Vt p-channel metal-oxide semiconductor (PMOS) and n-channel metal-oxide semiconductor (NMOS) transistors are used to leakage current in hold operation. i.e., M_PG1 and M_PG2 respectively.

Sleep transistors interrupt both PMOS and NMOS transistor networks from supply voltage or ground in state-destructive techniques. Gated VDD and gated-GND techniques are two types of gated VDD and gated-GND procedures. These two smart transistors can establish a virtual VDD and groun at top and bottom of inverter pair which can cut off the leakage path in standby mode as shown in **Figure 8**. The transistors in inverter pair have low-Vth to establish strong logic values at output nodes and these threshold voltages will effect on switching speed of memory cell. The pictorial representation of power gating technique based 6T topology SRAM cell is depicted in **Figure 8**. 14 nm FinFET based SRAM cell with power gating technique in different topologies such as 6T, 7T, 8T and 9T are shown in parts **(a)**, **(b)**, **(c)** and **(d)** of **Figure 9** respectively.

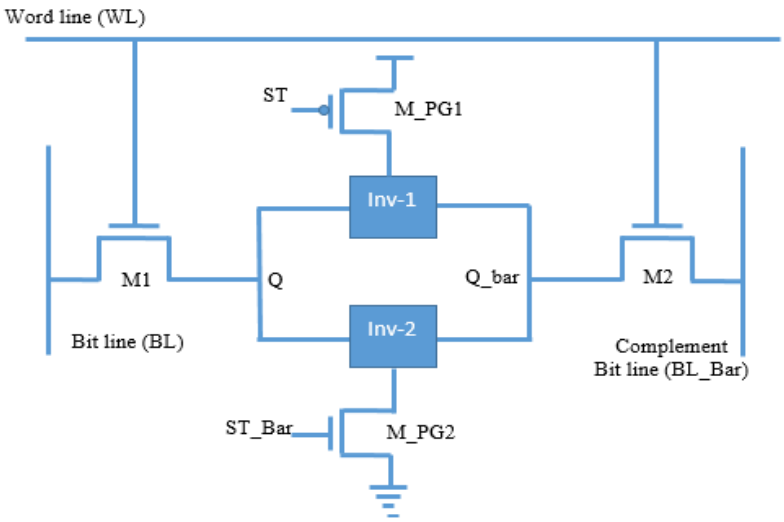
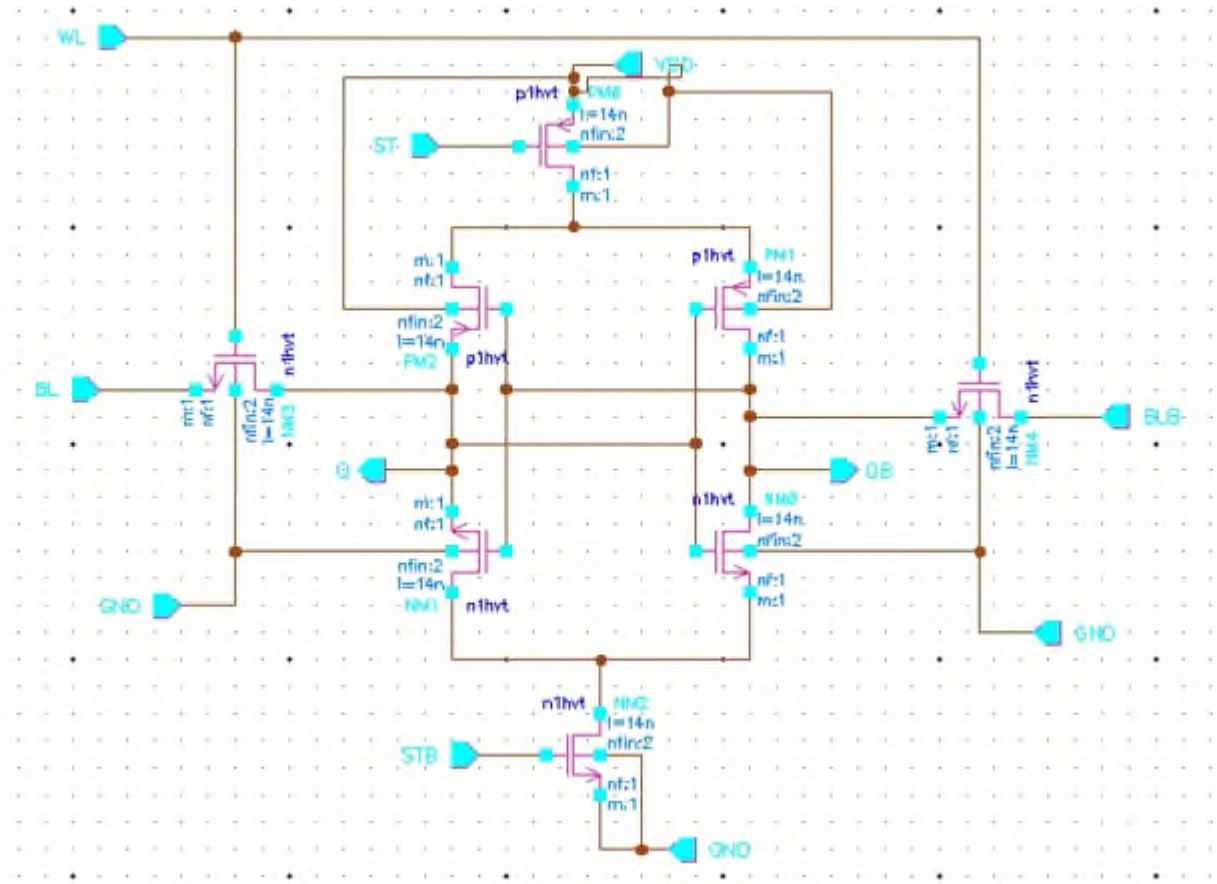


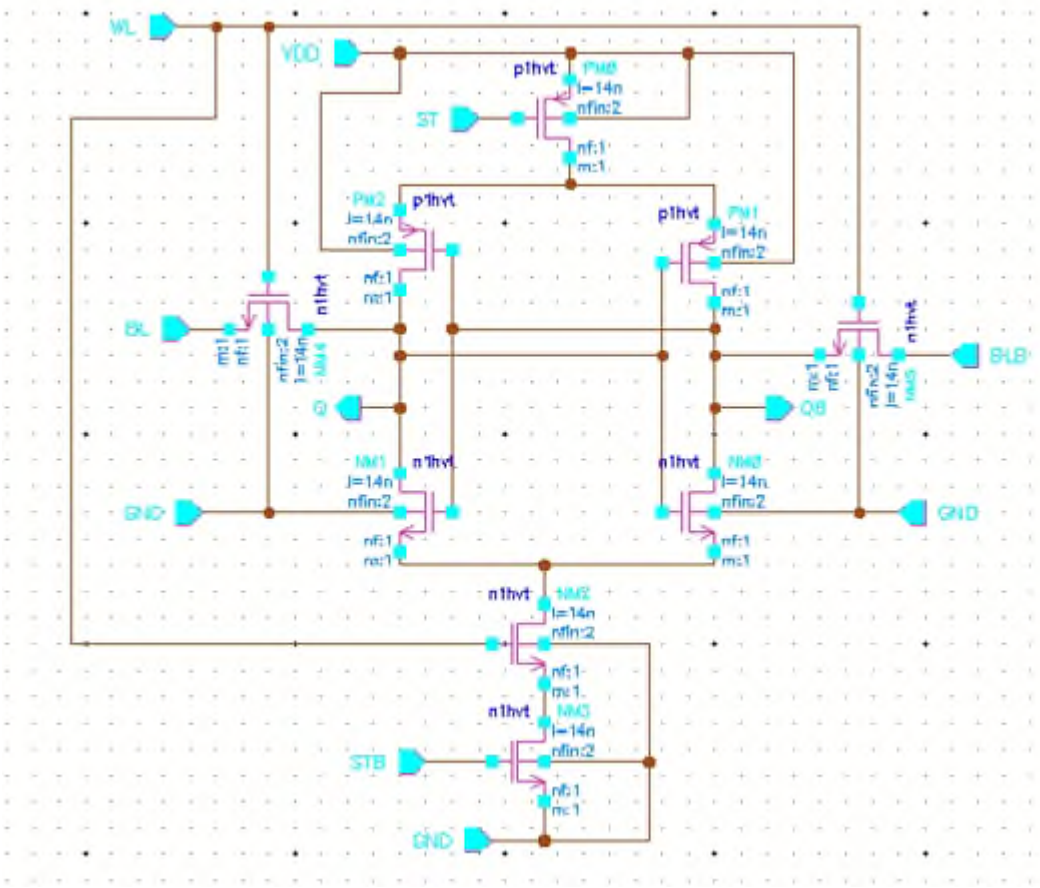
Figure 8. Power gating with sleep transistors based SRAM cell.

The speed transistor oriented power gating is incorporated in chosen four topology SRAM cells as shown in **Figure 9**. The sleep microelectronic technology drastically reduces discharge power during sleep mode by uninflected the logic networks utilizing sleep transistors and extra sleep transistors, on the other hand, increase the area and latency. Because the pull-up and pull-down networks have floating values, they can lose their status when sleeping. Because of the need to recharge transistors that lost status during sleep, these floating values have a significant impact on the awakening time and energy of the sleep strategy.



(a)

Figure 9. (*Continued*).



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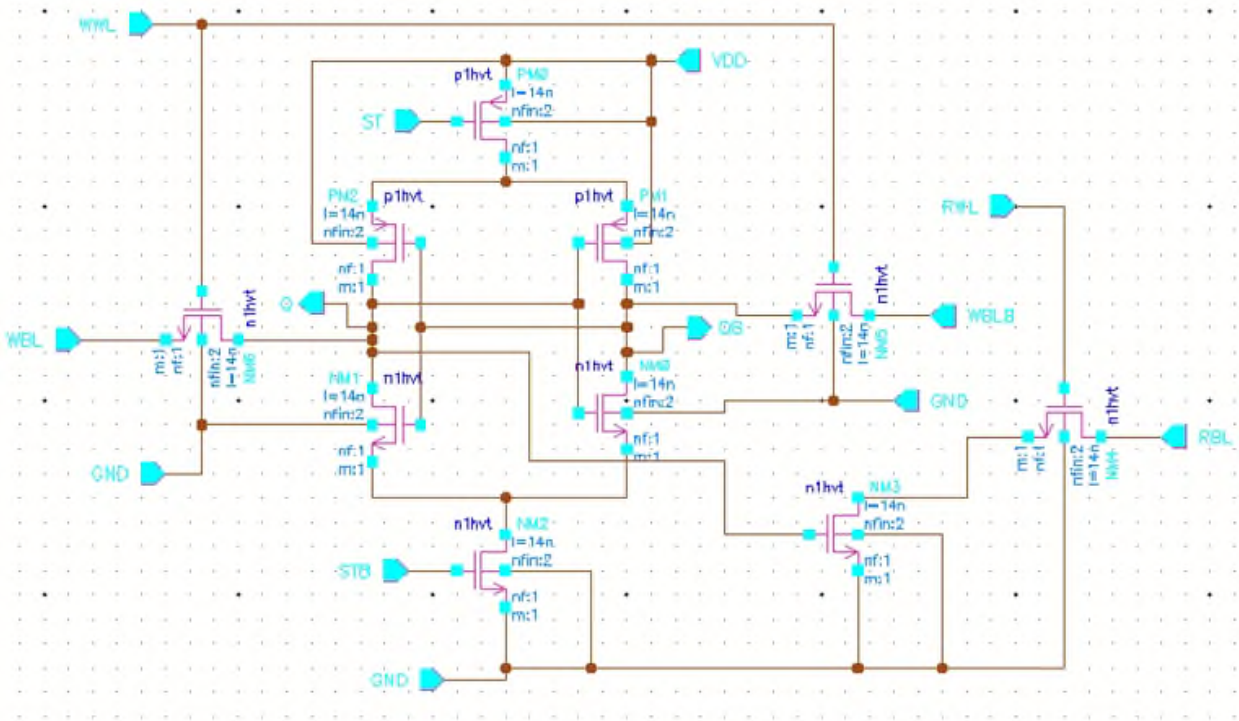

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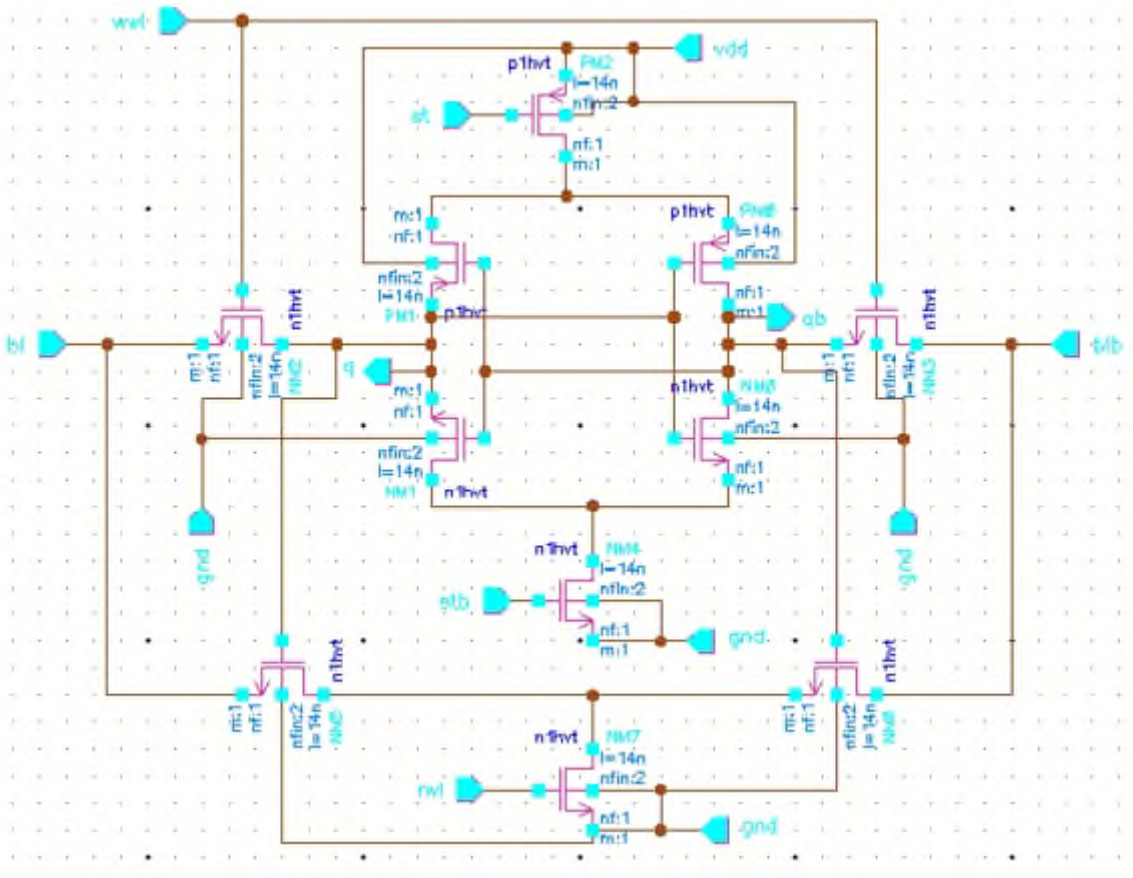
Figure 9. (*Continued*).



(d)

Figure 9. SRAM cells with power gating, **(a)** 6T cell; **(b)** 7T cell; **(c)** 8T cell; **(d)** 9T cell.

The performance analysis of SRAM cell using different power reduction techniques is shown in **Table 6** and the same is compared with existing methods. The results obtained from the later are shown **Table 7**.

Table 6. SRAM cells performance comparison with different power reduction techniques.

SRAM	Power dissipation (w)			Power delay product (ws)		
	Normal cells	With dynamic threshold	With power gating	Normal cells	With dynamic threshold	With power gating
6T	17.05 µw	23.51 nw	72.21 nw	163.68 fws	225.69 aws	690.32 aws
7T	15.22 µw	20.20 nw	43.99 nw	145.86 fws	193.59 aws	420.54 aws
8T	20.88 µw	33.22 nw	55.98 nw	244.96 fws	318.24 aws	532.16 aws
9T	25.57 µw	34.89 nw	62.78 nw	199.61 fws	333.54 aws	600.17 aws

Table 7. Comparison SRAM cells power dissipation with literature.

Parameter	Existing methods		Proposed work	
Power reduction techniques	Bit line floating[30]	Reverse body bias[31]	Dynamic threshold	Power gating
Transistor type	FinFET	FinFET	FinFET	FinFET
Technology (nm)	14 nm	14 nm	14 nm	14 nm
SRAM cell	6T, 8T	9T, 10T	Four Topologies (6T, 7T, 8T and 9T)	Four Topologies (6T, 7T, 8T and 9T)
SNM (mV)	345 mV	420 mV	483 mV	312 mV
Power (W)	102 µW	89 µW	34.89 nW	43.99 nW

5. Conclusion

The design and implementation of 14 nm FinFET centered memory cells have been enhanced through the strategic integration of power-saving techniques. Notably, the incorporation of dynamic threshold and power gating in SRAM cells has significantly contributed to boosting their performance and energy efficiency. The performance analysis conducted on SRAM cells with varying transistor counts, including 6T, 7T, 8T, and 9T configurations, has yielded remarkable results. The power dissipation in these designed SRAM cells has been effectively reduced by 20% compared to conventional cells. Furthermore, when compared to existing methods, the power savings achieved range between an impressive 77% and 79%, demonstrating the superior efficacy of the proposed strategies. One key aspect that sets these power-saving techniques apart is the substantial improvement in stability, which has led to a remarkable 13% increase. This heightened stability not only bolsters the reliability of the memory cells but also significantly enhances the overall data redundancy, particularly in low-power SRAM cell applications designed for bulk-sized memory systems. The outcomes of this study indicate that the amalgamation of dynamic threshold and power gating techniques offers a highly promising avenue for tackling power dissipation challenges in modern FinFET-based memory cell designs. The observed improvements in power efficiency, stability, and data redundancy hold significant implications for energy-conscious VLSI design applications, as well as for the broader semiconductor industry.

Author contributions

Conceptualization, MDR and YVN; methodology, MDR; software, MDR; validation, YVN and VVKDVP; formal analysis, MDR; investigation, MDR; resources, MDR; data curation, MDR; writing—original draft preparation, MDR; writing—review and editing, YVN and VVKDVP; visualization, MDR; supervision, YVN and VVKDVP. All authors have read and agreed to the published version of the manuscript.

Conflict of interest

The authors declare no conflict of interest.

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